**Amendments to the Specification**

Line 9 to line 29 on page 3 have been amended to read as follows:

Referring now to the first current path $I_A$, the current source transistor $M_1$ ~~is a PMOS transistor having~~ has a source terminal coupled to a supply signal VDD, a drain terminal coupled to a feedback control node A, and a gate terminal coupled to a central node B. The feedback transistor $M_4$ is an NMOS transistor having a drain terminal coupled to the feedback control node A, a source terminal coupled to a ground node, and a gate terminal coupled to a current mirror node C.

Referring now to the compensation current path $I_B$, the first resistor $R_1$ is coupled between the supply signal $V_{DD}$ and the central node B. The feedback control transistor $M_3$ is a PMOS transistor having a source terminal coupled to the central node B, a drain terminal coupled to the current mirror node C, and a gate terminal coupled to the feedback control node A. The feedback-generating transistor $M_5$ is an NMOS transistor having a source terminal coupled to the ground node, a drain terminal coupled to the current mirror node C, and a gate terminal also coupled to the current mirror node C.

Referring now to the second current path $I_C$, the output transistor $M_2$ is a PMOS transistor having a source terminal coupled to the supply signal $V_{DD}$, a drain terminal coupled to an output node $V_{REF}$, and a gate terminal coupled to the central node B. The thermal coupling transistor $M_6$ ~~is an NMOS transistor having~~ has a source terminal coupled to the ground node, and both a drain terminal and a gate terminal coupled to the output node $V_{REF}$. The second resistor $R_2$ and the output capacitor $C_1$ are coupled between the output node $V_{REF}$ and the ground node, such that the second resistor $R_2$ and the output capacitor $C_1$ are in parallel with the gate-source and drain-source voltages of the thermal coupling transistor $M_6$.